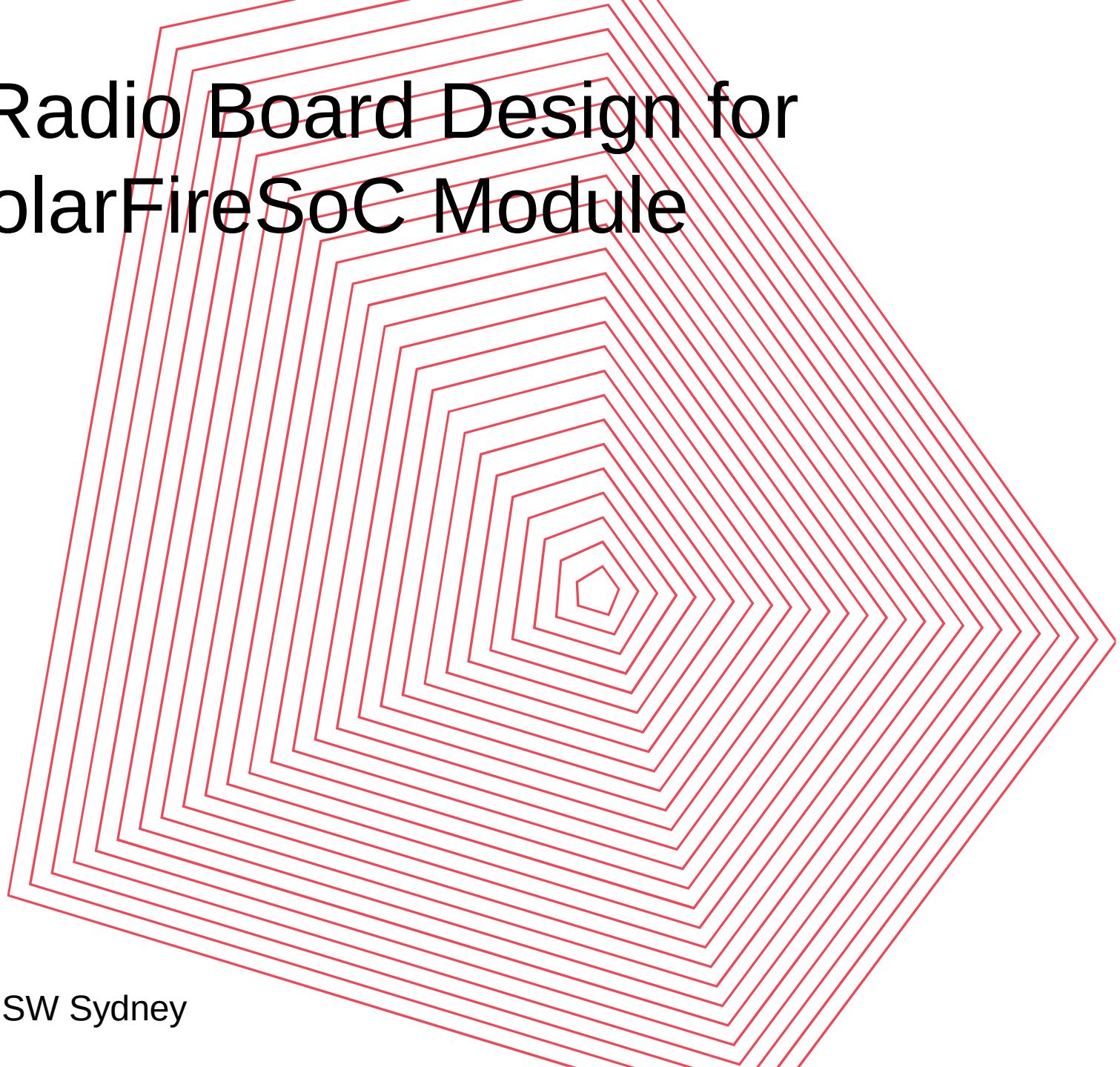
GNSS Radio Board Design for Aries PolarFireSoC Module

Karyn Nguyen



IGNSS 2022, UNSW Sydney

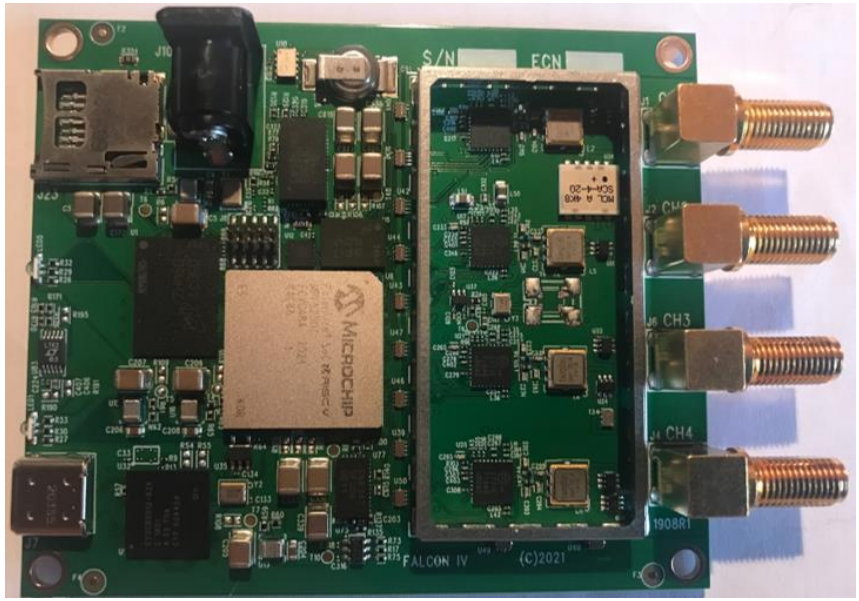
Thesis Project Aims

Reverse engineer current existing GPS FPGA receiver

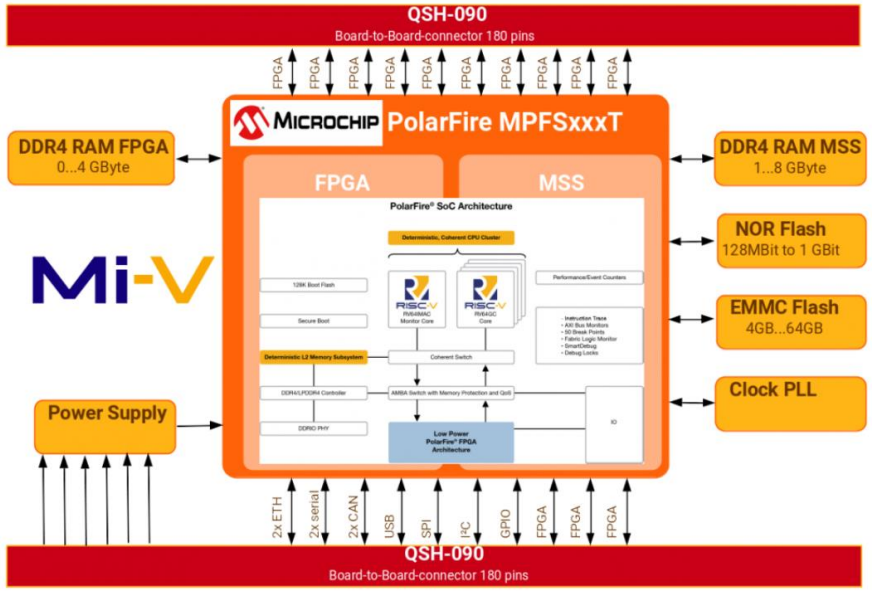
- Produce a workable design in Altium Designer

Design a unique board that can incorporate the existing RF front end with an Aries Embedded SoM unit

- Improvements on the current board to cater for more advanced applications (i.e. dual frequency reflectometry)
- Lower cost
- Easier to manufacture
- Use parts with better availability



Aries M100PFS SoM



PolarFire SoC FPGA

- MicroSemi MPFS250T

Main I/Os available:

- 5x multi-mode UARTs
- 2x I2C
- RTC
- GPIOs
- 2x Gigabit Ethernet
- 1x MMC 5.1 SD/SDIO

2x 16bit wide DDR4 RAMs

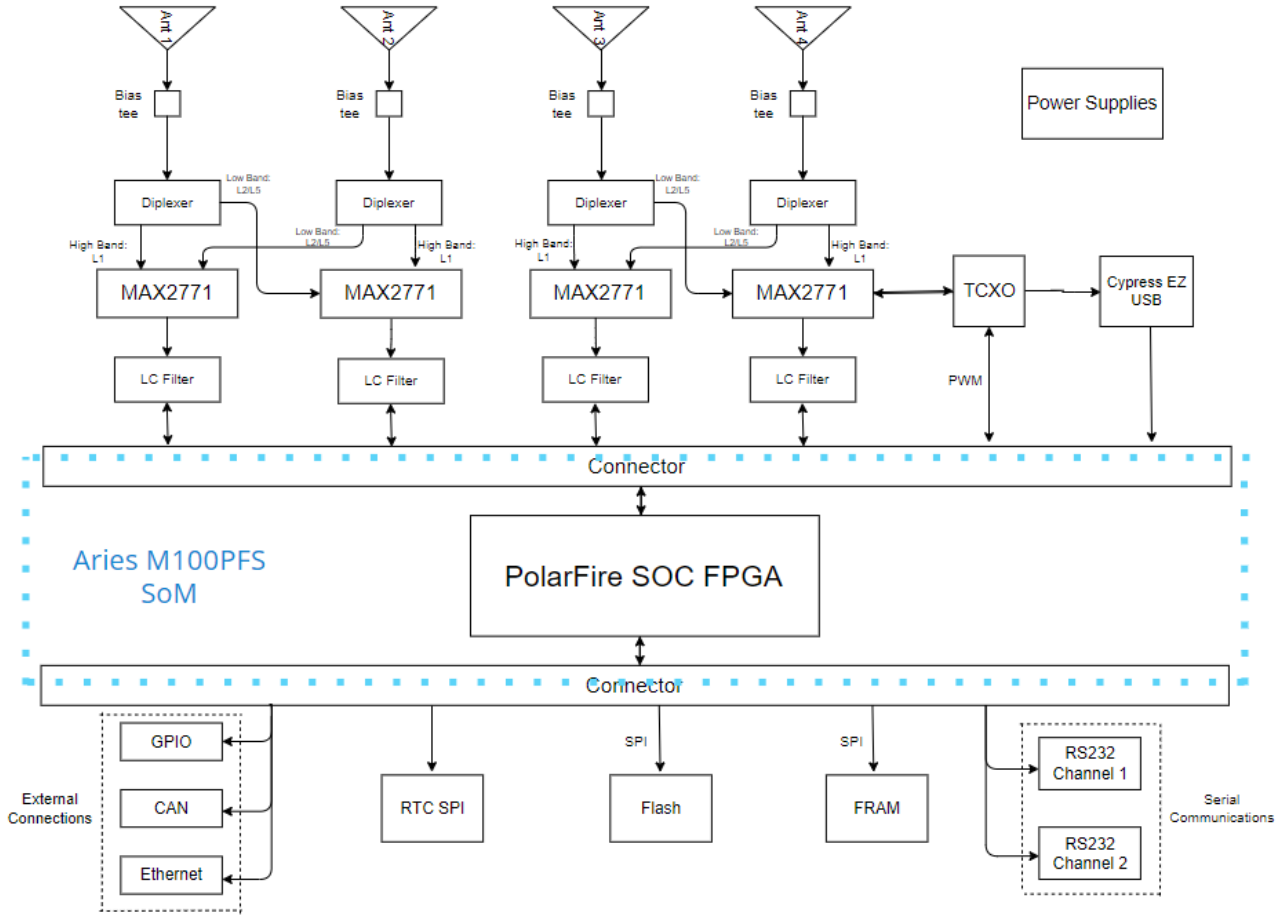
Power controlled by Dialog DA9063L-00, factory programmed to provide sufficient power for all subsystems on the Aries board

All connections are through two Samtec QSH-090-01-F-D-A connectors

High Level Block Diagram

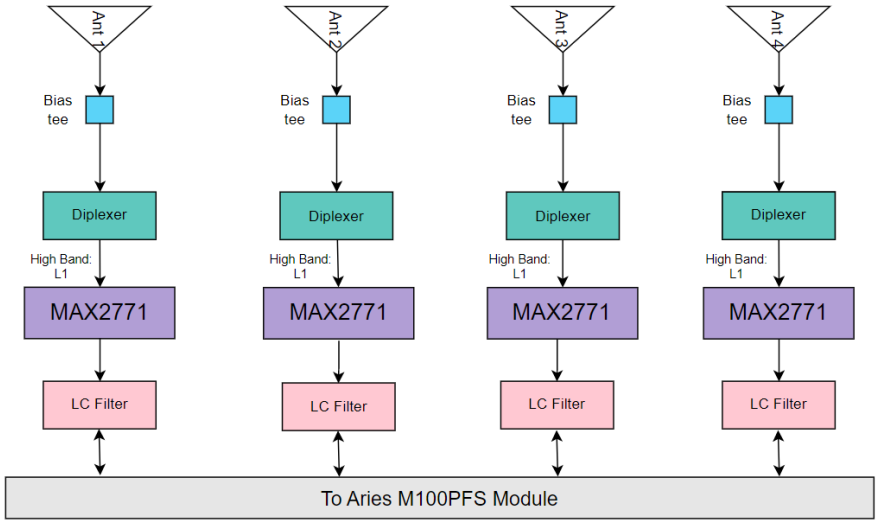
Simplified RF design compared to Falcon4 board

Supports 4 single frequency or 2 dual frequency antennas

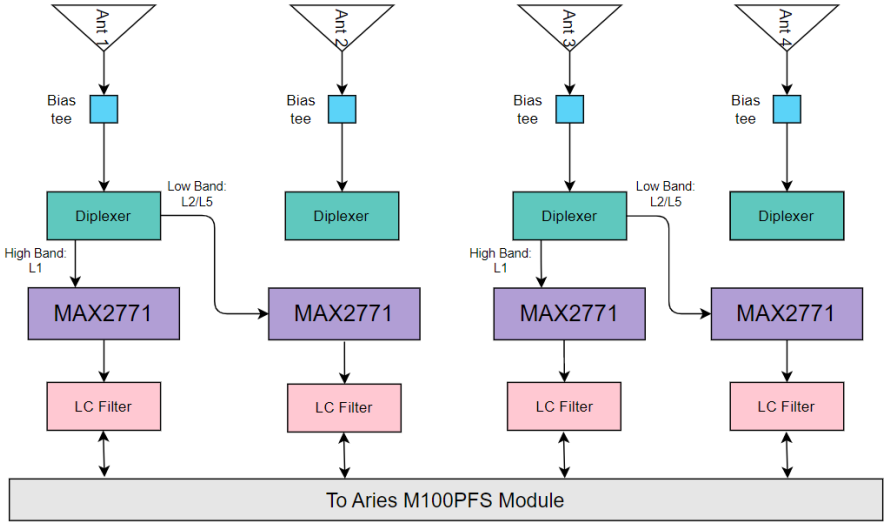


RF Front End Configurations

MAX2711s configured for four antenna single processing applications



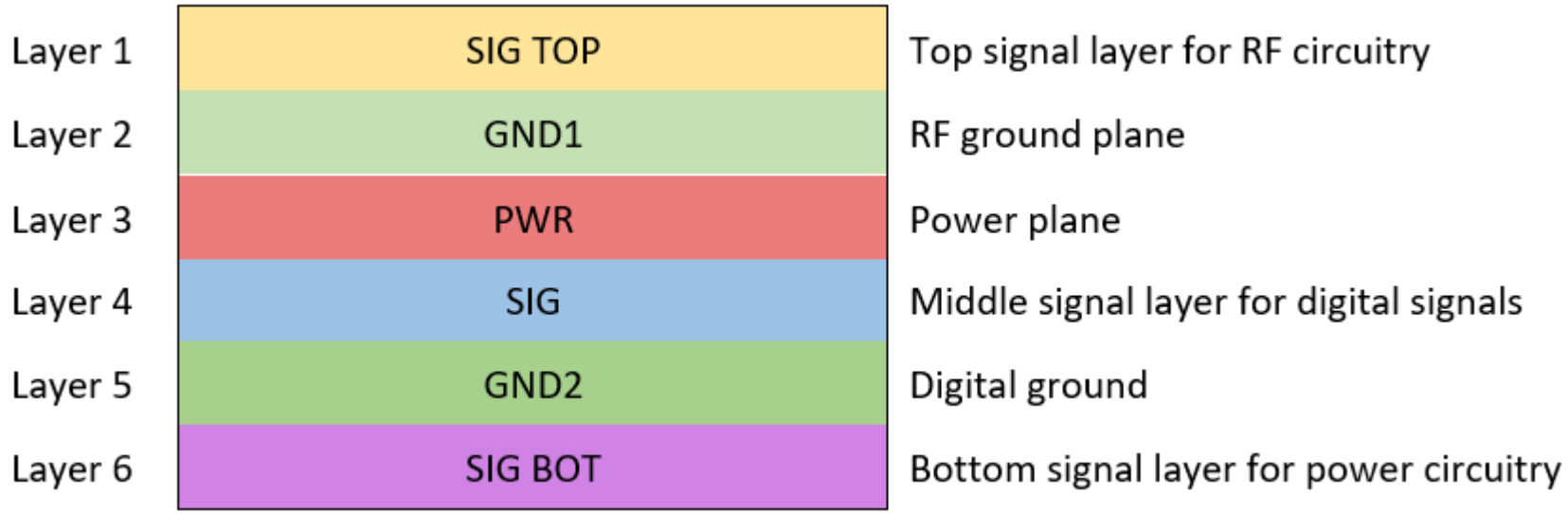
- MAX2711s configured for dual frequency – dual antenna processing applications



PCB Layer Stack-Up

6 layer board with ground planes splitting signal planes

Dedicated signal planes for power, digital and RF signals

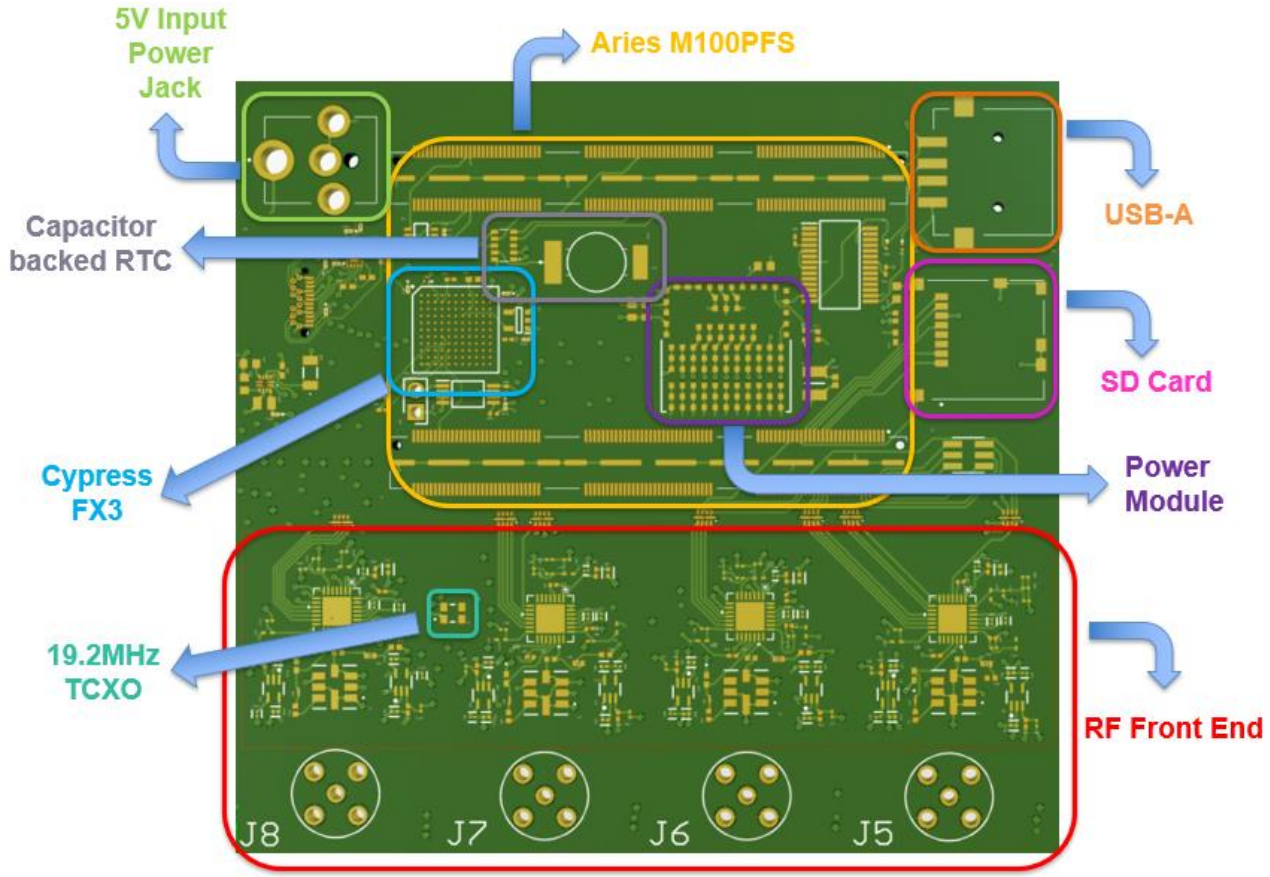


PCB Layout

96 mm x 90 mm PCB

1.6 mm thick

6 layer



Future Work

Board is currently being converted from Altium to KiCad

Plan to manufacture boards & replace the prototype with this design

Revisions could look into further cost reductions

Board revisions could also add the ability to connect RF outputs directly to USB3 chip thereby permitting the board to be used for IF data capture without needing the Aries SOM to be attached.

Board revisions could also look into adding an SSD to the design