Developing a new Australian GNSS Receiver using PolarfireSoc FPGAs

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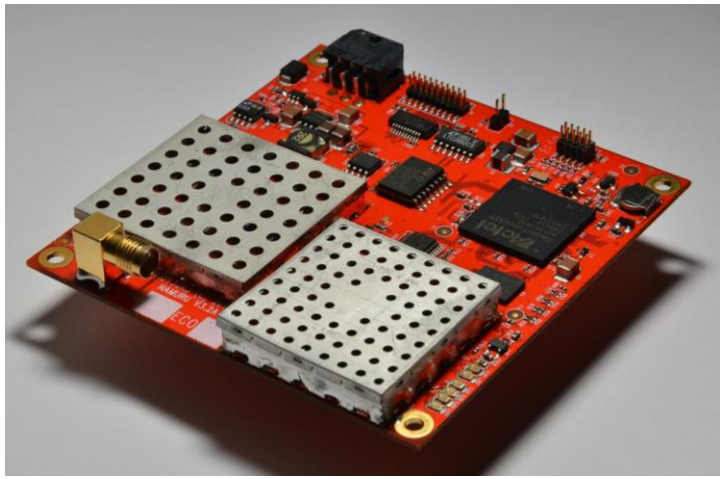
Namuru & Kea GPS Receivers

Enhancement of UNSW Namuru V3.2 that successfully navigated on the AFRL SHARC Cubesat

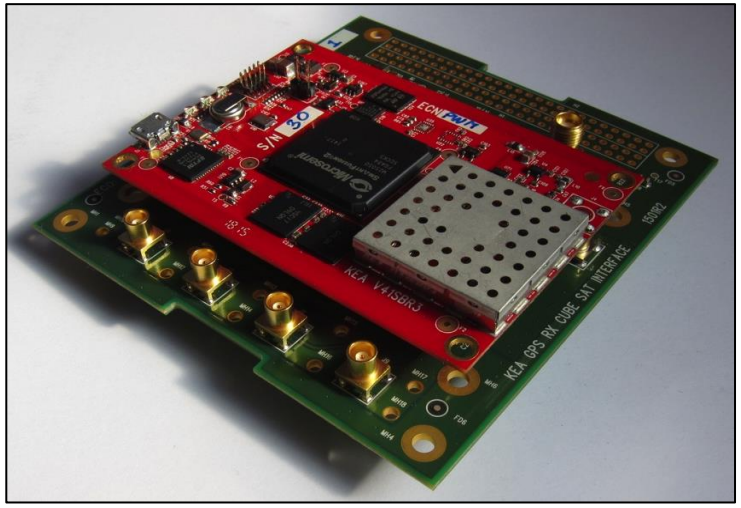
Namuru upgraded to Kea in 2015 by Embedded GNSS & General Dynamics Corp

Second fully Australian and New Zealand developed GPS receiver to navigate in orbit on board Buccaneer RMM

Commercially available through General Dynamics Corp in New Zealand



Namuru V3.2



Kea V4.1

New Applications & Upgrade Value Proposition

Kea was designed for Cubesat navigation

Unsuitable for GNSS remote sensing, multi-GNSS and high precision

- Single L1 RF front end => No good for GNSS reflectometry
- 100 MHz Cortex M3 processor => Too slow for multi-GNSS
- 1 Hz update rate too slow for high dynamics (eg. Rocket launch)
- 60k LE FPGA fabric too small for interesting applications

Very strong case for an upgrade

Australian Space Agency ISIEC grant application was successful

New GNSS Requirements

Process Galileo E1 and GPS L5 signals in addition to GPS L1 CA code

FPGA correlators capable of performing remote sensing (i.e. performing weak signal processing and generating small Delay Doppler Maps)

Much faster processor & much bigger FPGA

Fit into a PC104 (Cubesat envelope)

Perform dual frequency observations using two dual frequency antennas

Perform multiple single frequency observations using 3+ antennas

Capable of steaming outputs from RF front ends over a USB channel

Block Diagram

Using new Microchip Polarfire SoC

Five 600 MHz RISC-V cores

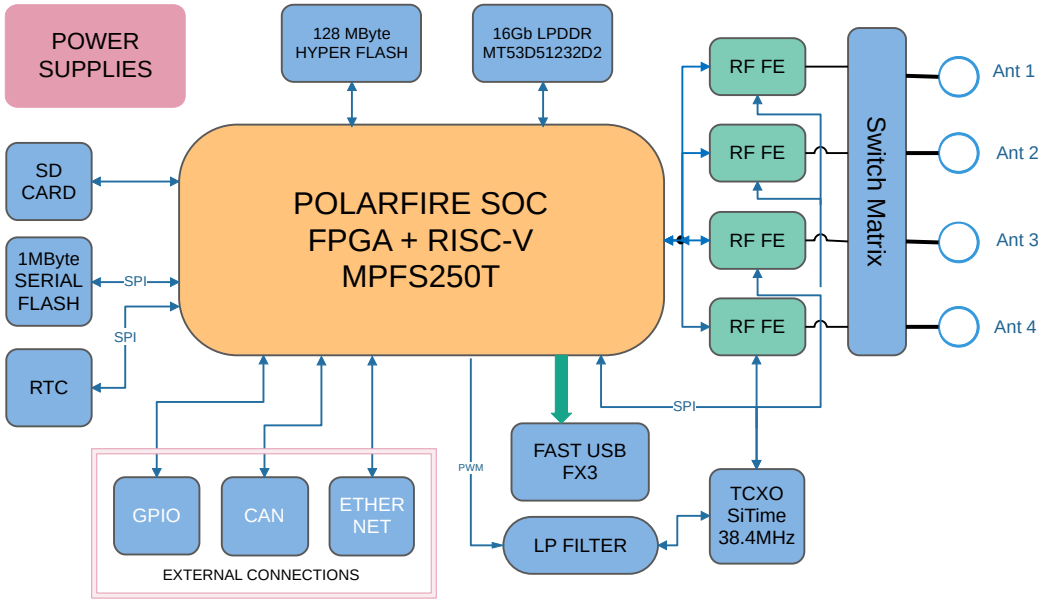
- One E51 integer supervisor core
- Four U54 floating point cores

250kE FPGA fabric

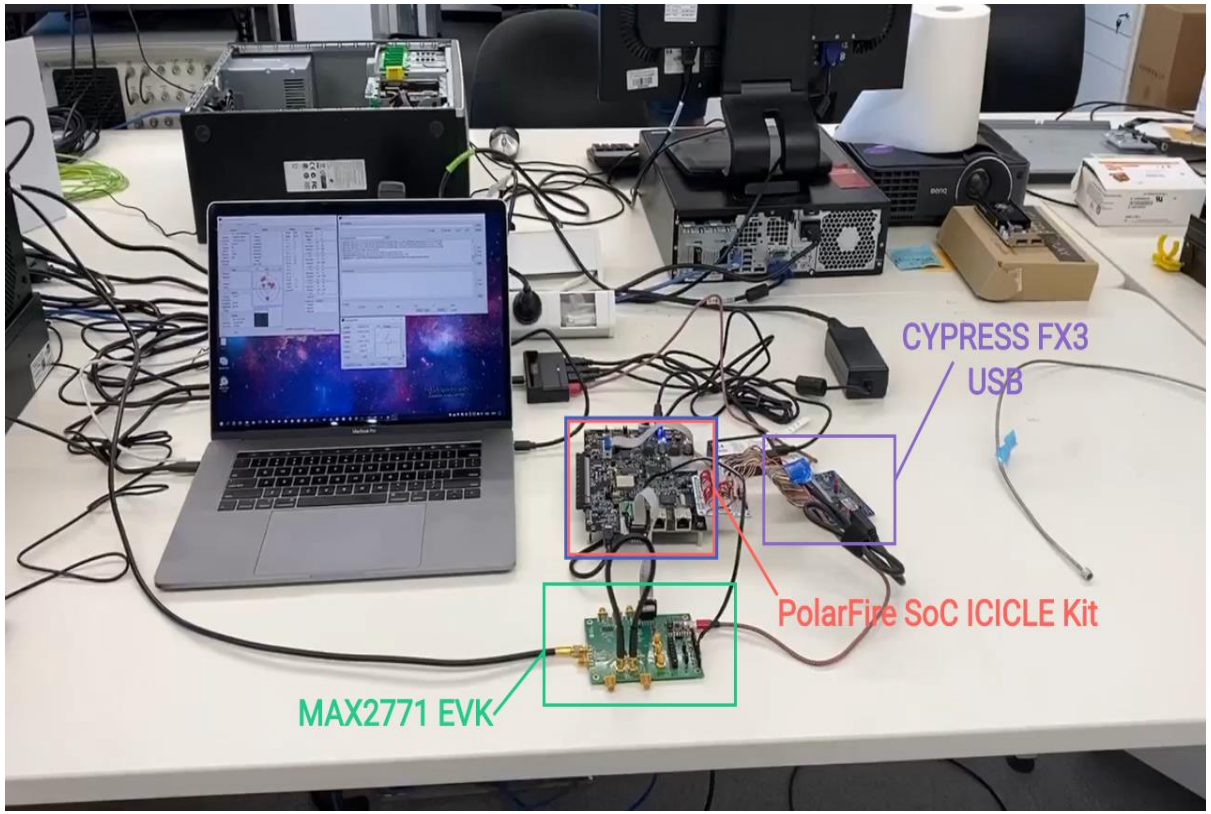
Four Max2771 GNSS front ends

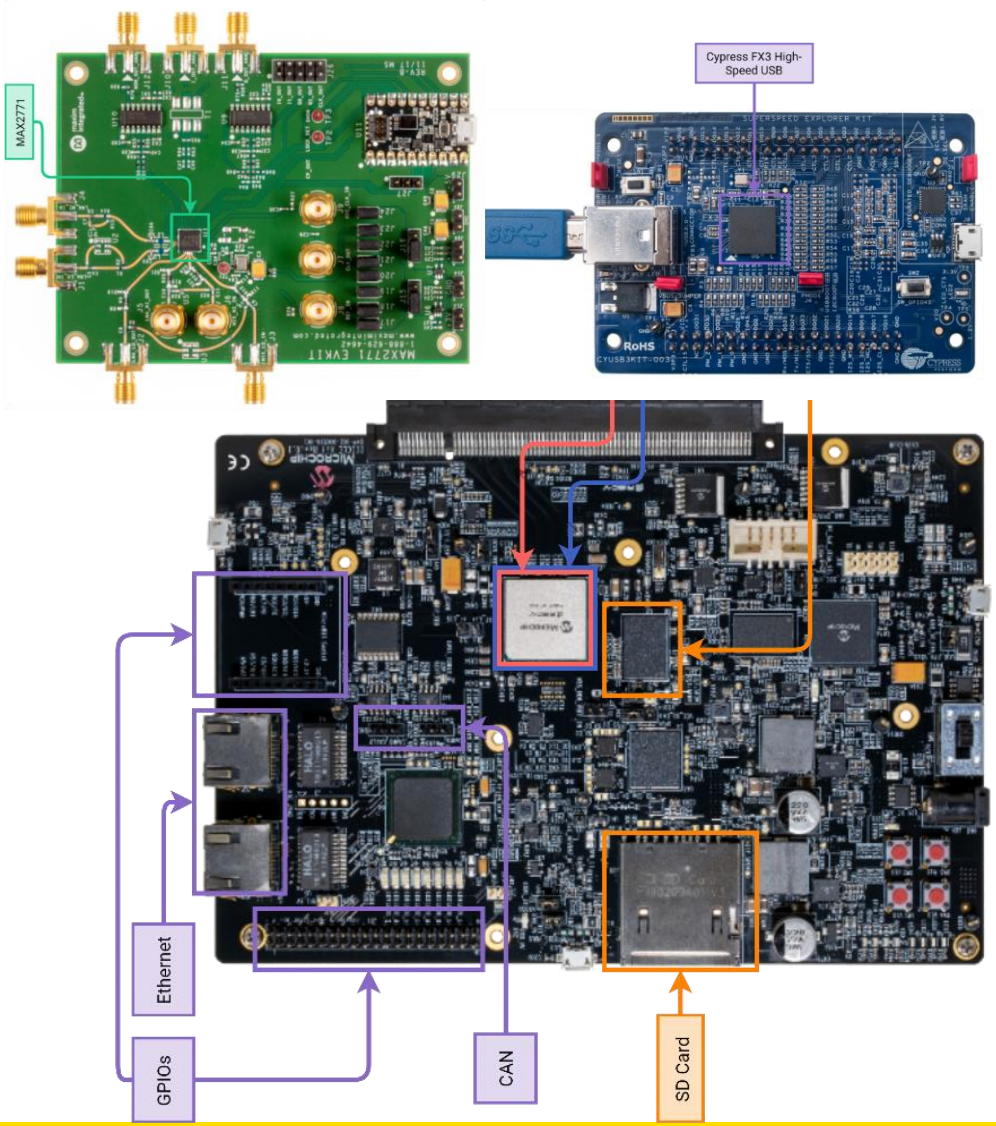
One Infineon CYUSB3014 USB3 chip

SEASKIP GNSS RX 2020 V4



Development System

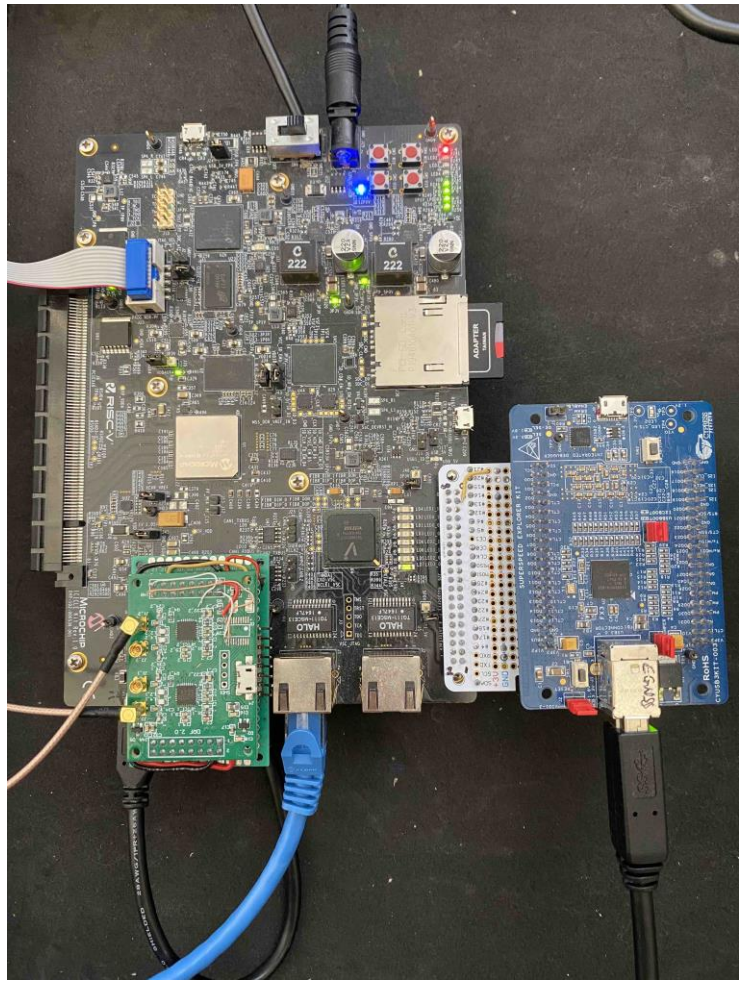




Improved Development System

Improved connection assemblies

Uses modified HelloGNSS RF front-end module



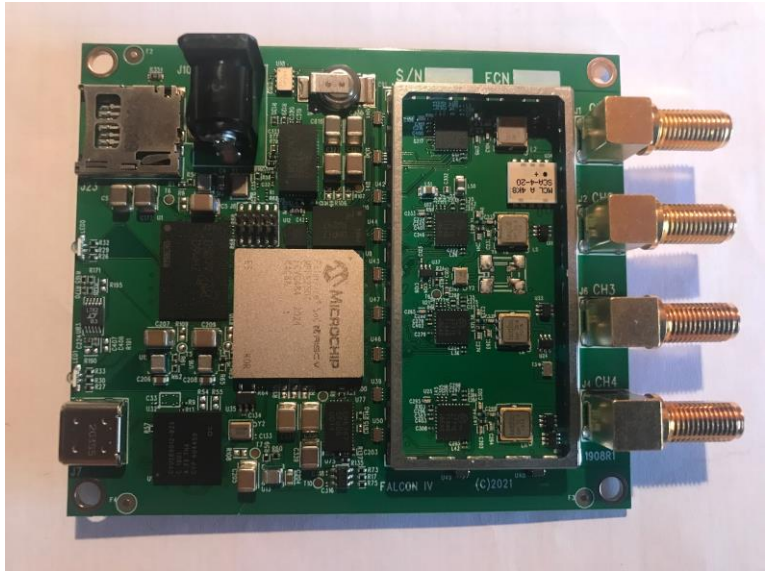
Falcon Four - Prototype One

Hardware designed and built by General Dynamics Corp in NZ

Two prototypes built – neither worked due to power supply and short circuit problems

Parts for a second prototype are being secured – long lead times caused by supply chain issues have delayed second board spin

Some power supply components have also been discontinued so those will be changed



FPGA & Firmware Development

This project mostly about FPGA and firmware development

Correlators reworked to do GPS CA code, Galileo E1 memory codes and GPS L5 codes, each with 4 FFT bins and 12 code phase taps per channel

Firmware modified to use Max2771 RF front ends

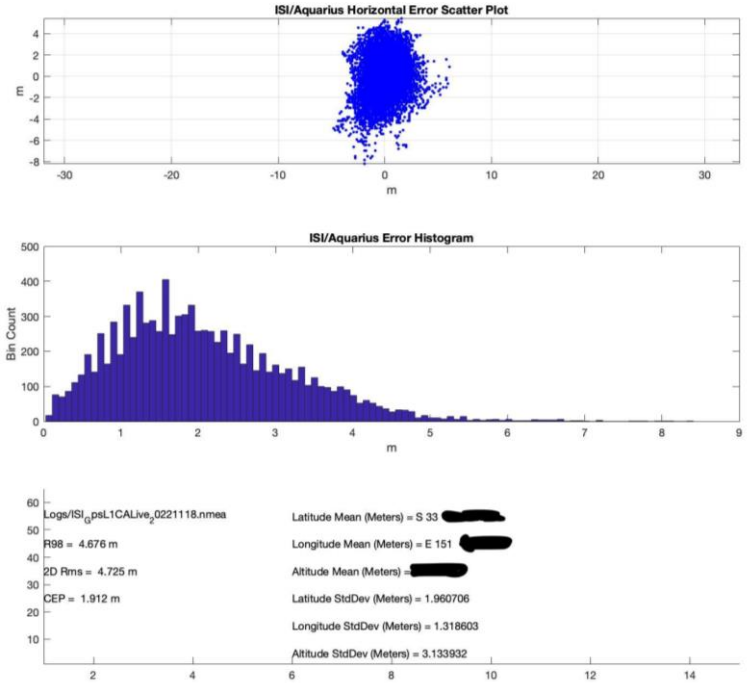
Firmware modified to process, extract and decode I/NAV and C/NAV data streams

Navigates with GPS C/A, Galileo E1 or GPS L5 signals

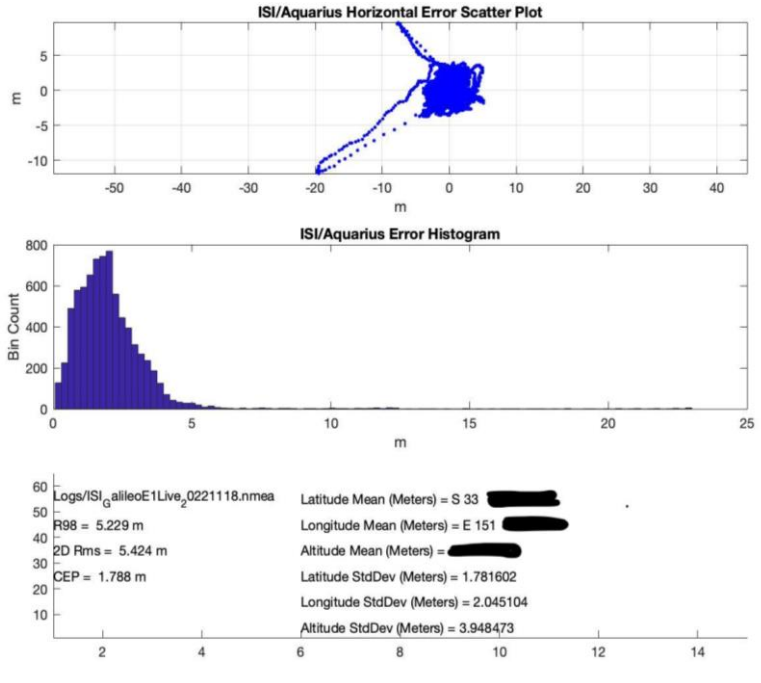
Position Scatter Plots

Galileo E1 and GPS L5 still not as good as GPS L1 C/A

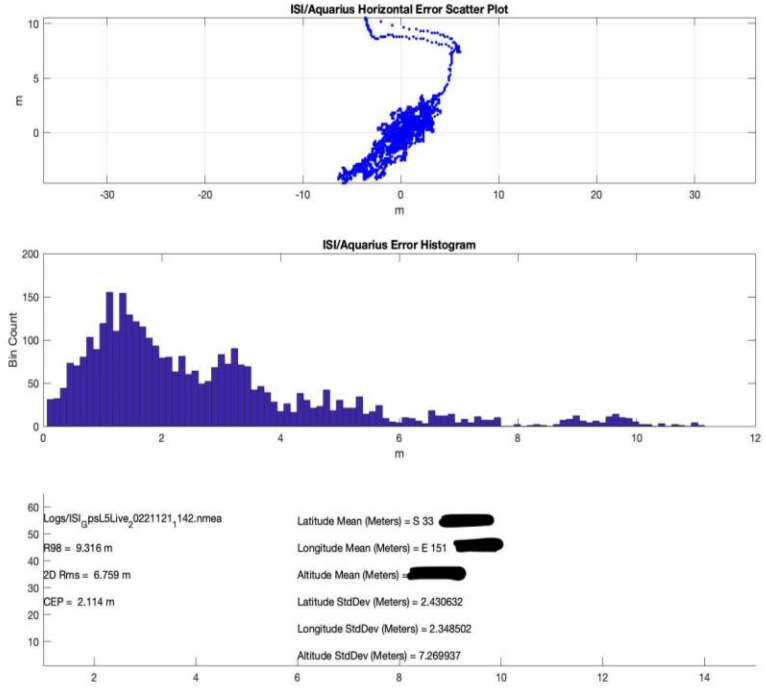
- Fewer Galileo and GPS L5 SVs and some firmware sync/data extraction issues



GPS C/A Code only



Galileo E1 only



GPS L5 Only

Development Team

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